Electronic Version
Stylesheet Version v1.1.1

SYSTEM AND METHOD FOR DIRECT WRITE TO DYNAMIC RANDOM ACCESS MEMORY (DRAM) USING PFET BIT-SWITCH

Abstract

2A control circuit for a memory array device having one or more memory storage cells associated therewith includes a true bit-line and a complementary bit-line coupled to the one or more memory storage cells. A sense amplifier is coupled to the true and complementary bit-lines, the sense amplifier being configured to amplify a small voltage difference between the true bit-line and the complementary bit-line to a full level signal at predetermined high and low logic voltage levels. A bit-switch pair selectively couples the bit-lines and said sense amplifier to fan-in circuitry, and is further configured so as to couple the fan-in circuitry to the true and complementary bit-lines prior to the activation of a wordline associated with a selected cell for a write operation thereto. Thereby, the write operation to the selected cell is commenced prior to the completion of time associated with signal develop-

ment on the true and complementary bit-lines.